Efficient Transient Compression Using an All-Silicon Nonlinear Transmission Line

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***Abstract*— Nonlinear transmission lines (NLTL's) have so far only been fabricated on GaAs. Here, an NLTL was monolithically integrated on a 2000-Ω·cm silicon substrate, demonstrating the applicability of the NLTL concept to silicon millimeter-wave integrated circuits (SIMMWIC's). The fall time of 74 ps of a 4-GHz sinewave was compressed to 32 ps at the output of the NLTL, in accordance with theory. This is the first working NLTL on silicon to our knowledge.**

***Index Terms*— Coplanar transmission lines, nonlinear wave propagation, pulse compression circuit, silicon.**

I. Introduction

NONLINEAR transmission lines (NLTL's) use the voltage-dependent capacitance of diodes distributed along a transmission line to introduce nonlinear wave propagation effects. The shockwave NLTL, as described here, steepens a leading or falling edge of a large time-domain signal, just like the wave-breaking effect of water in beaches [1]. NLTL's so far are available on GaAs with the best reported results being the generation of 480- [2] and 680-fs transients [3]. The realization of NLTL's on silicon has not been undertaken to the best of our knowledge.

While traditionally GaAs was the substrate chosen for monolithically integrated microwave circuits, high-resistivity silicon substrates with specific resistance over 1000 Ω·cm can also be used, as shown by many research groups [4], [5], for silicon millimeter-wave integrated circuits (SIMMWIC's). While SIMMWIC's with one-port devices (as oscillators or detectors) for frequencies up to 100 GHz were already demonstrated in 1988 [6], there are now new possibilities with Si–SiGe heterostructure bipolar transistors at frequencies above 30 GHz [7], triggering a growing demand for millimeter-wave components.

The major use of NLTL's will be in high-speed time-domain sampling, when integrated with diode sampling circuits, and potentially in high-order frequency multiplication. The advantage of GaAs compared to Si is the better carrier mobility and the higher breakdown field. Therefore, the minimum transients achievable on Si will be not as good as on GaAs. However, the excellent mechanical properties will allow the integration of active wafer probes using a micromechanical approach, resulting in short lines with negligible attenuation and dispersion to the device under test.

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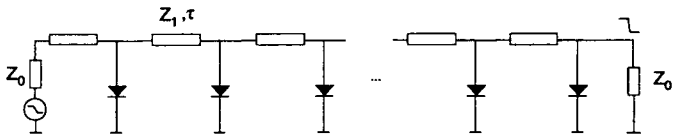

Fig. 1. Circuit diagram of an NLTL [1].

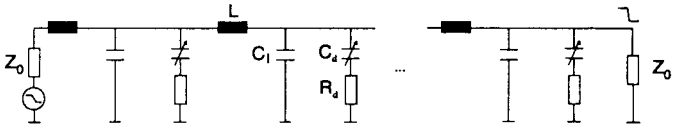

Fig. 2. Equivalent circuit of an NLTL [1].

The NLTL is monolithically integrated using a high-impedance coplanar waveguide (CPW) (with propagation velocity v_{CPW}) of impedance Z_1 and reverse-biased Schottky diodes serving as voltage-dependent capacitances, integrated periodically into the waveguide at spacings d. Fig. 1 shows the circuit diagram and Fig. 2 the equivalent circuit with $L = Z_1\tau$ and $C_l = \tau/Z_1$ being the line section inductance and capacitance, where $\tau = d/v_{\mathrm{CPW}}$. $C_d(V)$ and $R_d(V)$ are the diode capacitance and series resistance.

Taking into account the equivalent circuit parameters, it is possible to define the diode cutoff frequency

$$f_c = \frac{1}{2 \cdot \pi \cdot R_d(V) \cdot C_d(V)} \tag{1}$$

and the cutoff frequency of the line sections between two diodes

$$f_g = \frac{1}{\pi \cdot \sqrt{L[C_l + C_d(V)]}}. \tag{2}$$

When applying a large-signal voltage to the line the nonlinearity of the diode's capacitance, for uniform doping given as

$$C_d(V) = \frac{C_{j0}}{\sqrt{1 - V/V_{bi}}}, \tag{3}$$

will result in a bias dependent mean capacitance C_m. We calculated

$$C_m = \frac{C_{j0}}{\pi} \int_{-(\pi/\omega)}^{\pi/\omega} \frac{\cos^2 \omega t}{\sqrt{1 - \dfrac{V_0 \sin \omega t + V_A}{V_{bi}}}}\, d\omega t \tag{4}$$

with the applied voltage $V_0 \sin \omega t + V_A$ for a uniformly doped diode. This equation has been derived with the goal

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of impedance matching at the input of the transmission line and should not be confused with the large-signal capacitance derived by Landauer [8] to describe the propagation characteristics of shock waves.

With this mean capacitance a mean impedance of the line can be defined as

$$Z_L = \sqrt{\frac{L}{C_l + C_m}}. \tag{5}$$

For ideal matching this impedance should be as large as the load impedance $Z_L = Z_{\text{load}}$.

II. Design

A. Elevated CPW

To minimize the capacitance per unit length and the substrate effects of the waveguide, a fully elevated structure was designed. The parameters of the elevated CPW were calculated using mode-matching techniques. For a CPW 3 μm above the substrate, 100-μm ground-to-ground distance, and 20-μm center conductor width, we calculated an impedance of $Z_1 = 105\ \Omega$, an $\epsilon_{r,\text{eff}} = 2.7$, and an attenuation around 0.1 dB/mm at 50 GHz.

B. Diodes

High compression ratios in an NLTL depend critically on a high-capacitance swing of the diode, while still achieving a sufficient cutoff frequency and breakdown voltage.

To optimize the diode doping profile, we have extended the common model of uniform doping in the n^--region to include the possibility of doping steps. This allows us to optimize the $C(V)$ function and the series resistance, while maintaining an adequate breakdown voltage.

C. NLTL

Starting with the elevated CPW design described in Section II-A and the diode structure described above, we first derived the necessary diode spacing and the diode area from the target falltime $T_{f,\text{out}}$. The cutoff frequency f_g at the last section of the NLTL must be around

$$f_g = \frac{0.35}{T_{f,\text{out}}}. \tag{6}$$

The nonlinearity of the diode's capacitance should still be effective at the frequency f_g; this is why the cutoff frequency of the diode f_c should be around five times higher than f_g [1]. With the knowledge of the appropriate transmission line cutoff frequency f_g it is possible to calculate the distance d of the diodes as

$$d = \frac{c_0 Z_L}{Z_1 \pi f_g \sqrt{\epsilon_{r,\text{eff}}}}. \tag{7}$$

Then, the inductance of a section can be calculated as $L = Z_L/\pi f_g$ and with that the total capacitance $C_g = L/Z_L^2$. With $C_l = L/Z_1^2$ for the unloaded CPW line it is possible to get

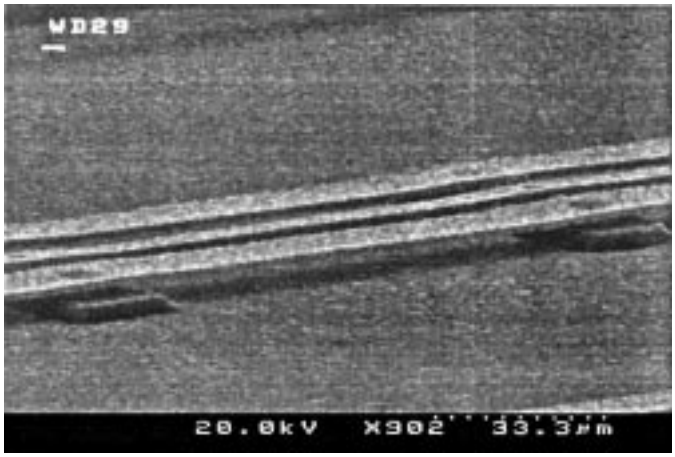

Fig. 3. SEM shot of a fully elevated CPW with diode pillar.

$C_m = C_g - C_l$. The next step is to determine the area of the diode A via the diode's reverse-biased capacitance:

$$C_{j0} = \frac{\epsilon_0 \epsilon_r A}{x_{j0}} \qquad \text{with} \qquad x_{j0} = \sqrt{\frac{2\epsilon_0 \epsilon_r}{q N_d V_{bi}}} \tag{8}$$

for a uniformly doped diode. C_{j0} is calculated from C_m [see (4)], the area A via the last equation.

III. Realization

A. Diodes

In compliance with our design a high-resistivity silicon substrate was implanted resulting in a doping concentration of $n^+ = 5 \cdot 10^{19}\ \text{cm}^{-3}$ at the surface. After that an epitaxial layer was grown at the Daimler–Benz Research Center in Ulm by MBE with a doping concentration of $n^- = 2.5 \cdot 10^{16}\ \text{cm}^{-3}$ and a thickness of 550 nm. Single diodes were fabricated on this material showing a breakdown voltage of 11 V, a capacitance swing of 2.1, and a cutoff frequency of 370 GHz. This is in good agreement with the theoretical values.

B. Airbridge NLTL

Because a comparable process to implant isolation on GaAs is not available on silicon and selective implantation was unavailable to us, a special process was developed. The wafer with n^+- and n^--layers is processed with a Pt–Au Schottky contact and a Ti–Au etch mask. The silicon is then etched twice using a KOH etch and the metal as masks, leaving diode pillars on a high-resistivity substrate. These pillars then support both the center conductor and ground conductor airbridges, using a two-resistlayer air-bridge process developed by us (see Fig. 3). As the span of the air-bridges is limited, passive pillars that are electrically isolated from the ground conductor are introduced.

IV. Results

On an NLTL with 40 diodes and 160 pillars (every fourth pillar is a diode) we observed an output signal of 1.6 V and a falltime of 32 ps from a 4-GHz 18-dBm sinewave input

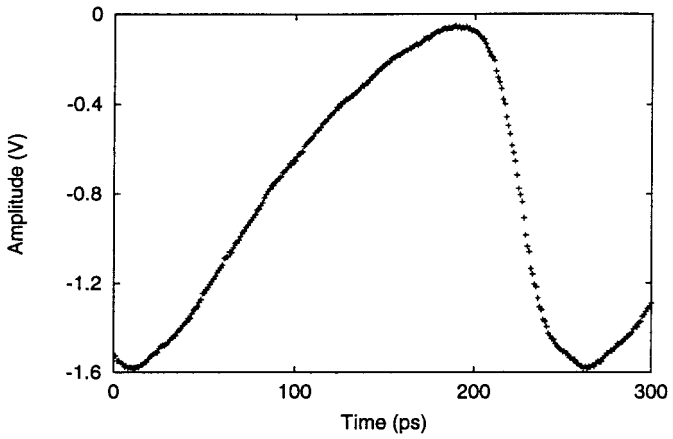

Fig. 4. Output signal of 40-diode NLTL on silicon with falltime of 32 ps, compressed from 74 ps (4-GHz sinewave).

(fall time 74 ps); see Fig. 4. For this measurement the system bandwidth was limited by a 26-GHz bias-tee. S-parameter measurements of the line showed an attenuation of 6.5 dB at 4 GHz. A problem to be faced in future was the large DC-resistance of the CPW of 18 Ω. The maximum reflection coefficient of the realized NLTL was 0.26.

V. Conclusions

We have demonstrated the first working NLTL on silicon substrates. A compression by 42 ps (74-ps input, 32-ps output) was observed on a 40-diode line, in accordance to theory. The realization has been undertaken using fully elevated coplanar waveguides. The next step is to optimize the NLTL to achieve a faster transient at the output. We therefore will fabricate NLTL's using optimized diode structures with a capacitance swing around 5, which should result in significant improvement in output transient time.

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